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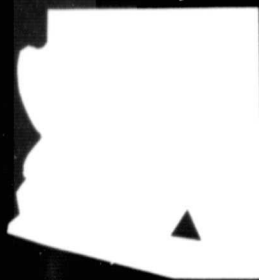
OPTIMIZATION OF CONTAMINATED OXIDE
INVERSION LAYER SOLAR CELL

JPL Contract No. 954189

by

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April 1976



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ABSTRACT

Contaminated oxide cells have been fabricated with efficiencies of 8.6% with values of $I_{sc} = 120$ ma, $V_{oc} = .54$ volts, and curve factor of .73. Attempts to optimize the fabrication step to yield a higher output have not been successful. The fundamental limitation is the inadequate antireflection coating afforded by the silicon dioxide coating used to hold the contaminating ions. Coatings of SiO_2 , therefore, were used to obtain a good antireflection coating, but the thinness of the coatings prevented a large concentration of the contaminating ions and the cells were weak. Data of the best cell were .52 volts V_{oc} , 110 ma I_{sc} , .66 CFF and 6.7% efficiency.

I. INTRODUCTION

A contaminated oxide cell consists of a single crystal silicon p-type wafer with an n layer induced in the top surface by a concentration of positive ions imbedded in a thermally grown oxide layer on the surface. The induced p-n junction thus formed has many of the properties found in a diffused junction. One of these is the presence of an electric field that can be used to separate hole-electron pairs created by external radiation. The photovoltaic effect operates in the induced junction as it does in a diffused junction. Contact with the inversion layer is made by diffusing donors in a finger pattern in the top surface of the wafer. A metal ohmic contact is made to conform to the finger pattern to carry away the current generated in the cell. A cross section of the contaminated oxide photovoltaic cell is shown in Fig. 1.

These cells have been successfully fabricated and yield 8.5% under artificial tungsten light at 140 mw/cm^2 at room temperature. These cells show a short circuit current of 120 ma (2 cm x 2 cm) and an open circuit voltage of .53 volts with a curve fill factor of .73. The internal resistance is .33 ohms. The V-I curve of a typical cell is found in Fig. 2. The fabrication steps are found in Appendix 1. They are more sensitive to an ultraviolet light than the conventional cell. The response to an ultraviolet fluorescent "black light" is 2.3 ma compared to 1.5 ma for the conventional "space cell". If all other factors affecting efficiency are the same or better for the contaminated oxide cell compared to the conventional cell and the response to the shorter wavelengths is greater, a higher efficiency cell should result. The object of this endeavor is to optimize the contaminated oxide cell to investigate the possibility of pushing the efficiency to the maximum.

II. CURVE FILL FACTOR

Several avenues of approach were investigated in the first part of this undertaking. First was an attempt to increase the curve fill factor so a greater current and voltage could be obtained at the maximum power point.

A process to coat the finger contact and the back contact with solder by solder dipping was developed. Good, uniform coatings of solder were obtained but after coating, the curve fill factor decreased and so did the efficiency of the cell. The problem stems from a higher resistance along the fingers despite the solder coating. The molten solder picked up a large portion of the silver on the contact and alloyed it into the solder. Thus, the thickness of the silver was reduced drastically. A substantial thickness of solder remained on top of the contact, but the resistance was more than the silver it removed. The total resistance therefore increased. Roughly, the resistivity of solder is ten times the resistivity of silver.

The resistance of the finger pattern can be decreased by increasing the thickness of the silver evaporation. Another approach is to electroplate a layer of copper on the fingers to increase the conductance. This evaluation has yet to be performed, although a technique for electrodepositing copper on the finger pattern has been developed.

III. ANNEALING

Since the diffusion step and the sodium impregnation step expose the wafer to high temperatures, an annealing step is necessary to reduce the imperfections in the wafer and thus increase the lifetime of the carriers in the wafer. An increase in collection of hole-electron pairs due to long wavelength photons results, and therefore an increase in the output current.

Experiments to determine an optimum annealing procedure were performed on wafers processed to yield contaminated oxide inversion layer solar cells. Prior to these experiments annealing was performed in the sodium furnace by quickly pulling the wafer to a position in the tube where the wafer was subjected to about 800°C. After 10 minutes at 800°C, the wafer was slowly pulled to around 500°C in an hour. It was found that the annealing step further added sodium to the oxide layer because of the residual sodium left in the tube after impregnation. Sodium deposited during the annealing tended to accumulate on the surface adding little to the inversion layer. Therefore, it was necessary that the impregnation step and the annealing step be separated. An old furnace was used for the annealing step. The mid temperature of the tube in the furnace was measured at 765°C and the end temperature at 473°C.

A group of four cells was prepared for sodium doping. All four were subjected to 1050°C for 5 minutes while the NaCl boat was present at the end of the hot zone at about 800°C. Nitrogen was flowing through the tube to carry the sodium chloride vapor to the wafers. After the 5 minutes, the wafers were quickly removed.

After the sodium treatment, the wafers were put in the 765°C zone of the annealing furnace and left for 1/2 hour, then removed quickly. No slow withdrawal was used. Subsequently they were metallized, etched and sintered. The results are as follows:

| <u>Cell No.</u> | <u>Isc (ma)</u> | <u>Voc (V)</u> |
|-----------------|-----------------|----------------|
| Na 49-1 | 120 | .52 |
| -2 | 105 | .51 |
| -3 | 100 | .50 |
| -4 | 115 | .51 |

These cells were fairly good, but not as responsive as could be expected overall.

Another experiment was performed to further judge the effect of the annealing procedure. Twelve wafers were processed identically up to the annealing step, all given a 10 minute sodium impregnation at 1050°C. Pairs of cells were annealed at 765°C for different periods of time. All of them were pulled quickly from the furnace. The following list represents the cell number, time of anneal at 765°C, short circuit current (I_{sc}) and open circuit voltage (V_{oc}) after completing cell.

| <u>Cell No.</u> | <u>Anneal Time (min.)</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (volts)</u> |
|-----------------|---------------------------|---------------------------------|------------------------------------|
| Na 51-3 | 10 | 112 | .51 |
| 4 | 10 | 122 | .50 |
| 5 | 20 | 120 | .52 |
| 6 | 20 | 100 | .51 |
| 1 | 30 | 115 | .52 |
| 2 | 30 | 122 | .53 |
| 7 | 40 | 110 | .51 |
| 8 | 40 | 125 | .52 |
| 9 | 50 | 125 | .53 |
| 10 | 50 | 125 | .54 |
| 11 | 60 | 125 | .54 |
| 12 | 60 | 130 | .54 |

From this experiment we find that annealing at the longer times has a slight benefit. At least 50 minutes is required to receive the maximum benefit.

Another annealing experiment was performed to see if a slow pull after an initial soak at 765°C would not yield optimum results. Four cells were processed together up to the annealing step, and then the annealing procedure was varied according to the following schedule. After an initial

soak at 765°C, different for each cell, they were all pulled slowly out of the furnace reaching 530°C in 1/2 hour.

| <u>Cell No.</u> | <u>Time of Initial Soak (min.)</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (V)</u> |
|-----------------|------------------------------------|----------------------------|---------------------------|
| Na 52-1 | None | 85 | .49 |
| 2 | 10 | 125 | .53 |
| 3 | 20 | 125 | .53 |
| 4 | 30 | 125 | .53 |

A ten-minute soak with a slow pull seems to be sufficient to obtain optimum annealing and will be used as the standard anneal.

The V-I curves of two of the cells in Experiment No. Na 52, namely, Na 52-1, and Na 52-2, are shown in Figures 3 and 4, respectively. In comparing these curves, an increase in both the short circuit current and the open circuit voltage can be seen. The annealing adds 40 ma to the 85 ma of the unannealed cell, and .04 volts to the .49 volts of the unannealed cell. An efficiency jump from 5.3% to 8.6% is also achieved by annealing.

IV. SODIUM IMPREGNATION

Since the amount of sodium in the oxide layer has a direct influence on the strength of the inversion layer, a test was performed to determine the effect that different time exposures to the sodium impregnation step would have on cell output. Four wafers were processed together up to the sodium impregnation step. Each one was then exposed to the sodium vapor in the furnace for a different length of time. The cells were then processed together to completion. The table below illustrates the schedule followed and the results.

| <u>Cell No.</u> | <u>Time in Furnace (minutes)</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (volts)</u> |
|-----------------|--------------------------------------|--------------------------------|-----------------------------------|
| 2 | 3 | 120 | .53 |
| 3 | 5 | 120 | .48 |
| 1 | 10 | 110 | .55 |
| 4 | 15 | 125 | .52 |

The wafers were placed in the furnace at a temperature of 1050°C, and the sodium chloride at a temperature of 800°C.

Very little overall change takes place as the time of exposure of the wafer to the sodium vapor is increased. Equilibrium is reached at least by three minutes in the furnace.

Since equilibrium is reached comparatively soon, perhaps a lower temperature would still allow sodium impregnation to occur but at a longer time. The furnace was set to 1000°C and another group of four cells processed the same as explained above. The results are shown below.

| <u>Cell No.</u> | <u>Time in Furnace (minutes)</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (volts)</u> |
|-----------------|--------------------------------------|--------------------------------|-----------------------------------|
| 1 | 5 | 71 | .51 |
| 2 | 10 | 80 | .47 |
| 3 | 15 | 80 | .51 |
| 4 | 20 | 100 | .52 |

It can be seen that time is a variable in the processing at 1000°C. The cell performance after 20 minutes exposure was less than the 3 minute exposure at 1050°C. Thus, the temperature seems to be critical in this crucial step.

Another run of eight cells was processed using a sodium impregnation temperature of 1100°C instead of 1050°C to determine whether a greater

cell output would result. The sodium boat was set in the furnace to a temperature of 800°C as in the other experiments above. The results of this run is found below.

| <u>Cell No.</u> | <u>Time in Furnace (minutes)</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (volts)</u> |
|-----------------|--------------------------------------|--------------------------------|-----------------------------------|
| 1 | 3 | 70 | .44 |
| 2 | 3 | 60 | .43 |
| 3 | 5 | 70 | .44 |
| 4 | 5 | 85 | .47 |
| 5 | 10 | 90 | .48 |
| 6 | 10 | 70 | .47 |
| 7 | 15 | 72 | .47 |
| 8 | 15 | 70 | .46 |

These cells are not giving the 125 ma I_{sc} and .52 volts V_{oc} that has been obtained with the wafers at 1050°C during the sodium step.

Temperatures lower or higher tend to produce cells of lower output and thus a near optimum temperature for sodium impregnation has been found to be about 1050°C. This has been the standard operating temperature for processing contaminated oxide cells, and therefore no increase in output or efficiency is expected by changing the temperature or time of exposure in the sodium impregnating step. A saturation seems to have been reached with respect to sodium concentration in the oxide layer and therefore the strength of the inversion layer is at the maximum using this method of impregnation.

V. OXIDE THICKNESS

The oxide layer used as a vehicle to hold the ionized sodium atoms also provides the anti-reflection coating. SiO_2 is not the best anti-reflection coating because the index of refraction is too low to make a

proper match between the silicon and air. Therefore, some losses are incurred because of reflection. Other losses occur because of the absorption of radiation in the SiO_2 layer.

To see if all of the oxide layer is necessary to hold a sufficient number of sodium atoms to create an adequate inversion layer, an experiment was performed to see the effect of thinning the contaminated oxide layer after sodium impregnation. A contaminated oxide cell was processed in the standard way. The I_{sc} was 95 ma and the V_{oc} was .5 volts. Photoresist was applied to protect the metal fingers and 1000 Å of oxide was etched away leaving 3600 Å. Measurements showed an I_{sc} of 90 ma and a V_{oc} of .49 volts. Another 1000 Å of oxide was removed leaving 2600 Å. The measurements were 95 ma and .5 volts. Again 1000 Å was removed to 1600 Å. A significant change was noted after the third etch, because an I_{sc} of 32 ma and a V_{oc} of .46 volts was found.

This experiment would indicate an independence of the thickness at least until 1600 Å is reached. Perhaps a thinner oxide will hold the same number of sodium atoms and thus the same inversion region but not attenuate the ultraviolet radiation as much and be a better anti-reflection coating.

Another experiment was performed to look at the output of the contaminated oxide cell as a function of the thickness of the oxide used to hold the sodium ions. Twelve wafers were processed together with only one variation in the processing. The original oxide step used as a mask for the finger diffusion, varied with each pair of wafers. The schedule is found below.

| <u>Cell No.</u> | <u>Oxide Thickness (A)</u> |
|-----------------|----------------------------|
| 1 & 2 | 3000 |
| 3 & 4 | 4000 |
| 5 & 6 | 5000 |
| 7 & 8 | 6000 |
| 9 & 10 | 7000 |
| 11 & 12 | 8000 |

All wafers were given the same annealing and sodium impregnation steps. The results are found in Table I.

There is a variation with oxide thickness that would indicate an optimum thickness about 4000 A. This is the standard processing thickness used for cells fabricated before. No clear increase in cell output can be gained by changing the oxide thickness from the standard process.

TABLE I

| <u>Cell No.</u> | <u>Oxide Thickness (A)</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (volts)</u> | <u>UV (ma)</u> |
|-----------------|------------------------------------|--------------------------------|-----------------------------------|--------------------|
| 1 | 3000 | 85 | .49 | 3.0 |
| 2 | 3000 | 75 | .48 | 2.9 |
| 3 | 4000 | 100 | .49 | 3.1 |
| 4 | 4000 | 110 | .41 | 2.9 |
| 5 | 5000 | 65 | .48 | 2.7 |
| 6 | 5000 | 75 | .47 | 3.0 |
| 7 | 6000 | 90 | .50 | 3.2 |
| 8 | 6000 | 96 | .51 | 3.2 |
| 9 | 7000 | 83 | .48 | 3.1 |
| 10 | 7000 | 82 | .49 | 3.1 |
| 11 | 8000 | 80 | .48 | 3.1 |
| 12 | 8000 | 90 | .48 | 3.0 |

VI. SILICON MONOXIDE LAYERS

Contaminated oxide solar cells were fabricated by impregnating sodium into a layer of silicon monoxide deposited on a silicon wafer. The silicon monoxide layer was evaporated in a vacuum to a thickness sufficient to yield the characteristic purple color of the antireflection coating on conventional cells. The sodium impregnation procedure was the same as the one for silicon dioxide. A pattern consisting of nine fingers over the 2 cm width of the cell was used as the front contact. The fabrication steps were as follows:

Clean

Thermally grow diffusion mask oxide (4000 \AA)

Photoresist and etch for diffusion

Diffuse phosphorus (POCl_3) 945°C 15 minutes

Remove dioxide

Deposit SiO

Sodium impregnate SiO (1050°C) (NaCl at 800°C)

Anneal

Photoresist and etch SiO

Metallize

Photoresist and etch metal for contact

Sinter

Measure

Four cells in experiment NaSiO-1 were processed. Cells 1 and 2 were processed using the steps listed above. The sodium impregnation was deleted on Cell 3. Cell 4 was a normal SiO_2 contaminated oxide cell with a nine finger pattern.

Short circuit current (I_{sc}), open circuit voltage (V_{oc}) and response to an ultraviolet source (u.v.) were measured for each of the four cells. The results are found in the following table.

| <u>Cell</u> | <u>I_{sc} (ma)</u> | <u>V_{oc} (volts)</u> | <u>u.v. (ma)</u> |
|-------------|---------------------------------|------------------------------------|------------------|
| 1 | 110 | .52 | 3.0 |
| 2 | 100 | .50 | 3.5 |
| 3 | 86 | .50 | 1.4 |
| 4 | 100 | .51 | 3.5 |

The I-V characteristic curve for Cell 1 is shown in Fig. 5. The curve factor is very small. This is partly due to the comparatively high resistance of the inversion layer and the nine finger pattern. The short circuit current and open circuit voltage show that the cell is responding fairly well, but a high resistance is hindering a higher output.

A definite difference is noted between the contaminated and non-contaminated oxide cells, showing that the sodium impregnation does cause a stronger inversion layer and therefore a higher current. The ultraviolet response for the contaminated cells is also much higher showing the benefit of the shallow induced junction and the high electric field aiding the photovoltaic action.

Another batch of cells was fabricated using the 30 finger pattern instead of the 9 finger pattern in an attempt to achieve a better curve factor. This was Run #Na-SiO-2. The steps used during fabrication are the same as for the previous run. Figure 6 shows the I-V characteristic curve obtained for one of the cells. The open circuit voltage (.52 volts), short circuit current (110 ma) and response to u.v. (3.6 ma) have changed but little, but the curve factor (.66) was greatly improved.

The object of using SiO instead of SiO₂ as the medium to carry the contaminating ions, was to increase the short circuit current because the SiO affords a better antireflection coating than SiO₂. The thickness for an effective antireflection coating is about 800 Å. In order for a strong inversion layer to be induced in this thin layer, the sodium contamination concentration must be stronger than the concentration was in the SiO₂ layers because a decrease in output was noted for thicknesses of 1600 Å in SiO₂.

In order to assess the affect of SiO thickness on the output of the contaminated silicon monoxide cell, an experiment was performed. Two cells were processed with the SiO processing explained above. The thickness of the coating on the first cell was designed to produce the first blue interference color (~700 Å) and the thickness on the second cell to produce the second blue color. This experiment was designed to see if a thicker SiO coating would still produce an adequate antireflection but allow more contaminate, and therefore produce a stronger inversion layer.

The results show less output for the thicker oxide. An I_{sc} of 100 ma and a V_{oc} of .49 volts was obtained for the thicker oxide. A greater difference was found in the ultraviolet response, 4.2 ma for the first cell and 1.9 ma for the second. The V-I curves for these two cells are found in Figures 7 and 8. The curve factors are still inadequate, probably due to a weak inversion layer.

Another series of cells was processed in an attempt to get better curve factors and higher short circuit currents. After sintering, the four cells processed had short circuit currents of 102 ma to 110 ma and open circuit voltages of .49 to .51 volts. The curve factors were better than the SiO cells processed before. Figures 9 and 10 show the characteristic

curves of two of the cells. These two cells were packaged and sent to JPL.

Data on Cell #1 and #3 are listed below.

Data on Cell No. 1

| | |
|------------|---|
| Light | Incandescent source equivalent to 140 mw/cm^2 |
| T | Room Temperature |
| I_{sc} | 110 ma |
| V_{oc} | .51 volts |
| I_{mp} | 93 ma |
| V_{mp} | .37 volts |
| CFF | .61 |
| Power Out | 35 mw |
| Efficiency | 6.2% |

Data on Cell No. 3

| | |
|------------|-----------|
| I_{sc} | 102 ma |
| V_{oc} | .49 volts |
| I_{mp} | 90 ma |
| V_{mp} | .36 volts |
| CFF | .65 |
| Power Out | 33 mw |
| Efficiency | 5.9% |

The thickness of the oxide layer does not allow a strong contamination of sodium atoms and therefore weak inversion layers are produced with high surface resistances and low curve factors.

VII. PHOSPHORUS CONTAMINATION

Sodium has been used as the main contaminate for the inversion layer solar cell. Sodium chloride was used in the contaminating furnace to supply the contaminate to the oxide. Other substances might work as well, however, and to show this, a batch of cells was fabricated with the same procedure used in fabricating the contaminated oxide cell found in Appendix 1 except phosphorus chloride was used instead of sodium chloride for the contamination step. All of the cells were between 110 ma and 115 ma I_{sc} and between .49 and .53 V_{oc} . The I-V characteristics of the cell with the highest power output when exposed to 140 mw/cm² incandescent radiation is found in Fig. 11. The data for this cell are:

| | |
|----------|-----------|
| I_{sc} | 115 ma |
| V_{oc} | .53 volts |
| I_m | 108 ma |
| V_m | .41 volts |
| CFF | .73 |
| Eff. | 8.7% |
| UV Light | 3 ma |

These data show results as good as cells fabricated with sodium contamination.

VIII. DISCUSSION

Almost every attempt to increase the efficiency of the contaminated oxide cell by changing fabrication steps has shown a decrease or an independence on power output. The process used to produce cells before an attempt to optimize has, so far, been the optimum process. Different anneals, different oxide thicknesses, different contact metals, different coatings, different contaminants, different sodium impregnation times and temperatures have all had a negative or no effect on the cell efficiency. If the contaminated oxide cell is compared to a conventional cell, many of the parameters are similar. The open circuit voltage of .54 volts for a 10 ohm-cm wafer is similar to the conventional diffused junction cell. The .73 curve factor is also similar. The short circuit current is lower, however, while typical values of 140 ma for a 2x2 cm cell exposed to 140 mw/cm² is found in the conventional cell, only 120 ma for the same size and radiation is found for the contaminated oxide cell. If 140 ma could be reached by the inversion layer cell, other things remaining the same, the efficiency could reach 10% or higher.

A large portion of the difference in short circuit current is due to the dioxide layer being a poorer antireflection coating than the monoxide layer, but the monoxide being too thin to provide an adequate vehicle for large contamination.

The experiment with phosphorus instead of sodium shows that other substances can be used for contamination. Perhaps a substance can be found to give the proper index of refraction for good antireflection properties and still produce a strong inversion layer at the surface.

Appendix 1

Steps in Fabrication of Contaminated Oxide Cell

1. The wafers are cleaned by scrubbing with a Q-tip. Acetone and isopropyl alcohol are used. After a deionized water rinse, the wafers are blown dry with N_2 .

2. A 50-minute oxidation at 1100°C follows. Wet oxygen, produced by bubbling O_2 through a bubbler, is passed down the furnace tube at .3 L/min in a 3" tube. The water in the bubbler is hot. An oxide coating of about 5000 Å is grown. A dry oxygen flow is also present at .8 L/min. Wafers are inserted and removed rapidly.

3. A standard photoresist procedure is used to cut holes in the oxide for diffusion. Pattern used is the finger pattern.

4. Diffusion occurs at 945°C for 15 minutes. Phosphorus derived from nitrogen bubbling through $POCl_3$ is used as the dopant. The $POCl_3$ temperature is maintained at 14°C . The flowrate of N_2 through the $POCl_3$ is .2 L/min, of N_2 direct is .6 L/min and O_2 direct at .6 L/min. The wafers are inserted and removed rapidly.

5. The oxide on the wafers are then impregnated with sodium by exposing the wafer to 1050°C for 10 minutes with sodium chloride vapor being carried down the tube with flow of N_2 . The sodium chloride is set in a boat in the tube at the edge of the furnace.

6. After the sodium impregnation, the wafers are taken to another furnace set at 760°C . Annealing takes place by soaking at 760°C for 1/2 hour and pulling 2" per 10 min for 5 pulls to 500°C .

7. The wafers are briefly dipped in a 48% solution of HF. This removes the thin oxide in the diffusion areas but leaves about 4000 Å over the p areas.

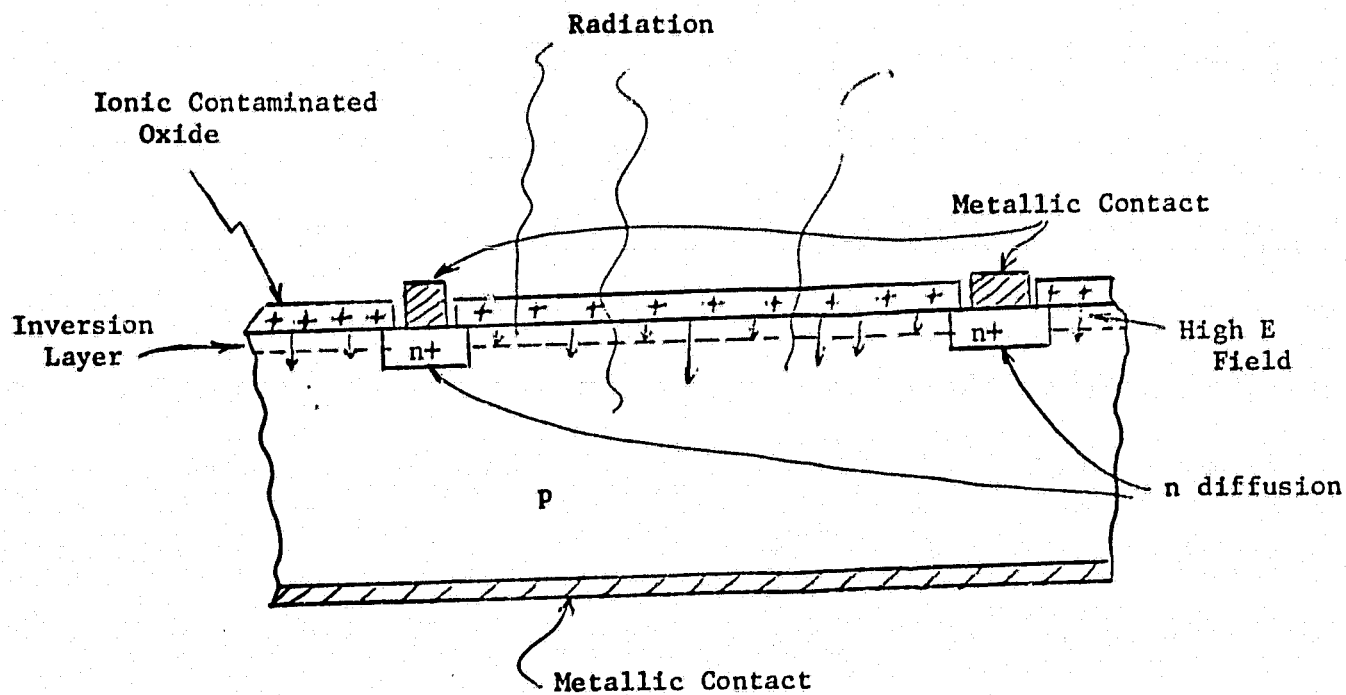
8. A deposit of Ti-Ag is evaporated on the top surface of the wafer. Evaporation takes place at 10^{-5} mm Hg.

9. Finger pattern is etched into the metal coating by a photolithograph process. The layer of silver is etched with a 1:1 nitric and water solution. The titanium is etched by a 114, 21, Litre' (by weight) solution of Ammonium Persulphate, sodium fluoride and water. The latter solution is heated to 60°C when used.

10. A protective wax coating is applied to the top of the wafers and are subjected to a Si etch that removes the n diffused layer from the bottom and sides of the wafers.

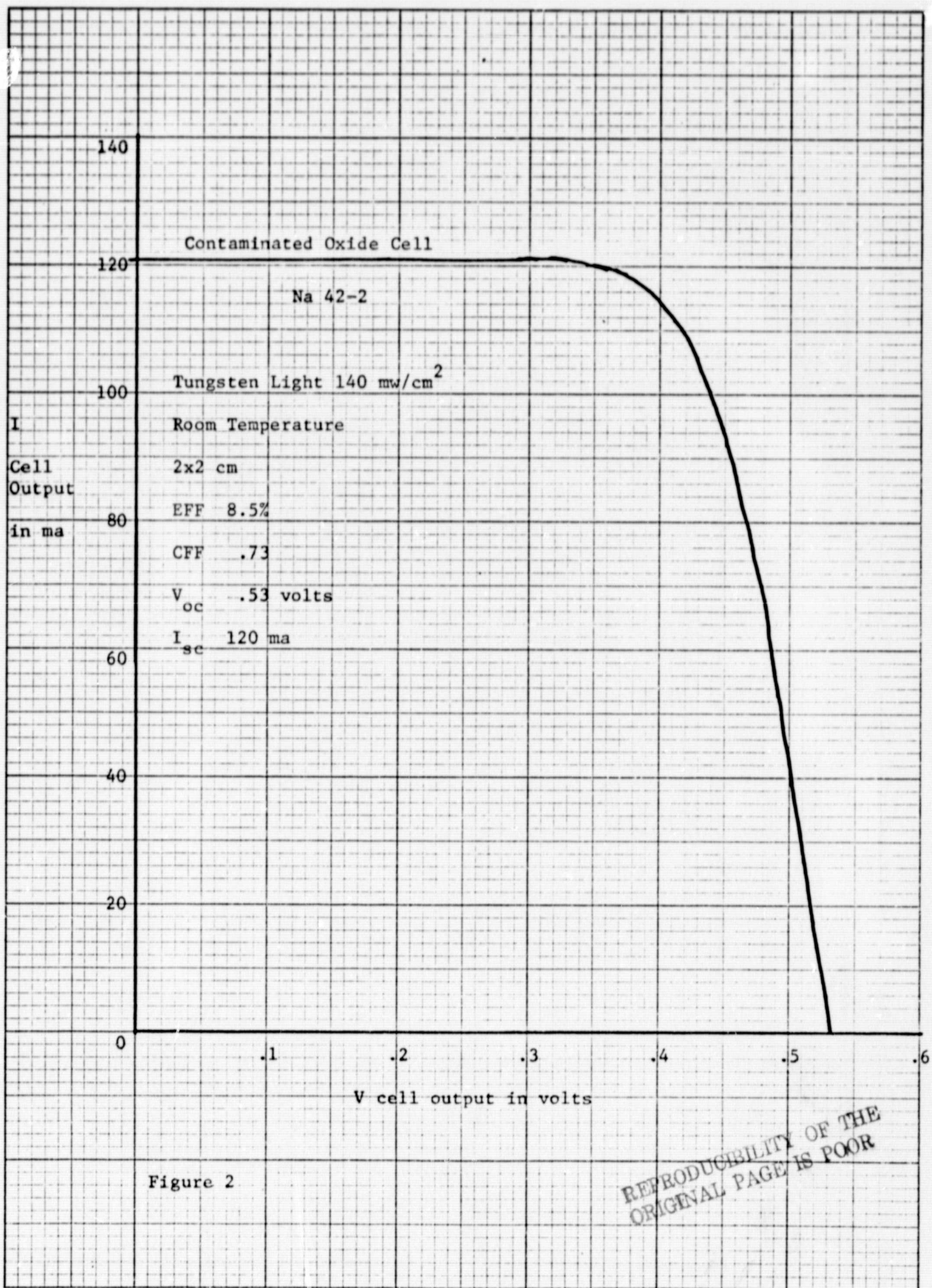
11. An evaporated layer of Ti-Ag is applied to the back.

12. The wafers are sintered at 520°C for 5 minutes under an atmosphere of forming gas.



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Figure 1 Cross-section of Contaminated Oxide Cell



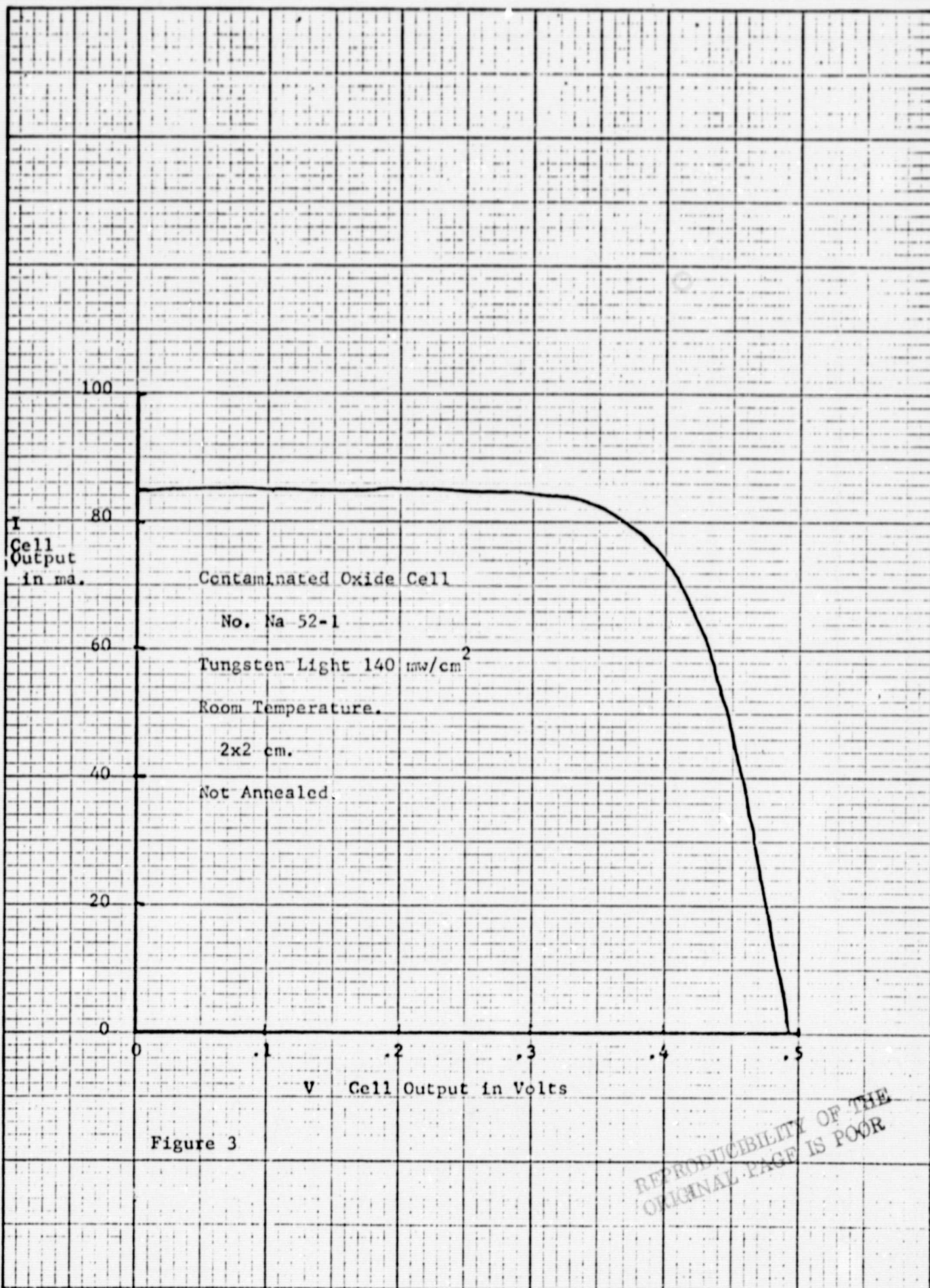


Figure 3

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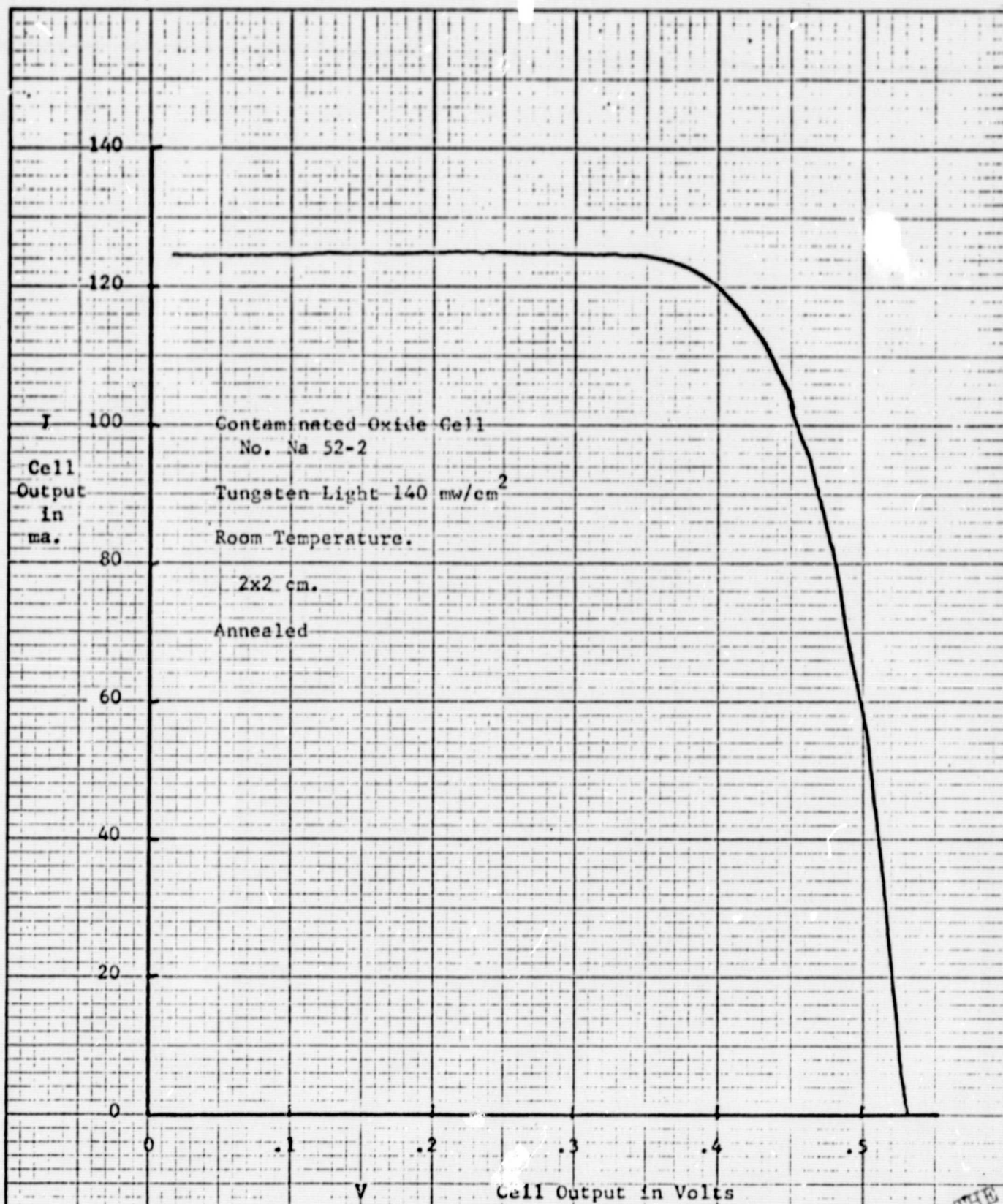


Figure 4

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MADE IN U.S.A.
KEUFFEL & ESSER CO.

Cell
Current
Out
ma

120

100

80

60

40

20

0

.1

.2

.3

.4

.5

Contaminated SiO Cell Na-SiO-1 Cell 1

9 finger pattern

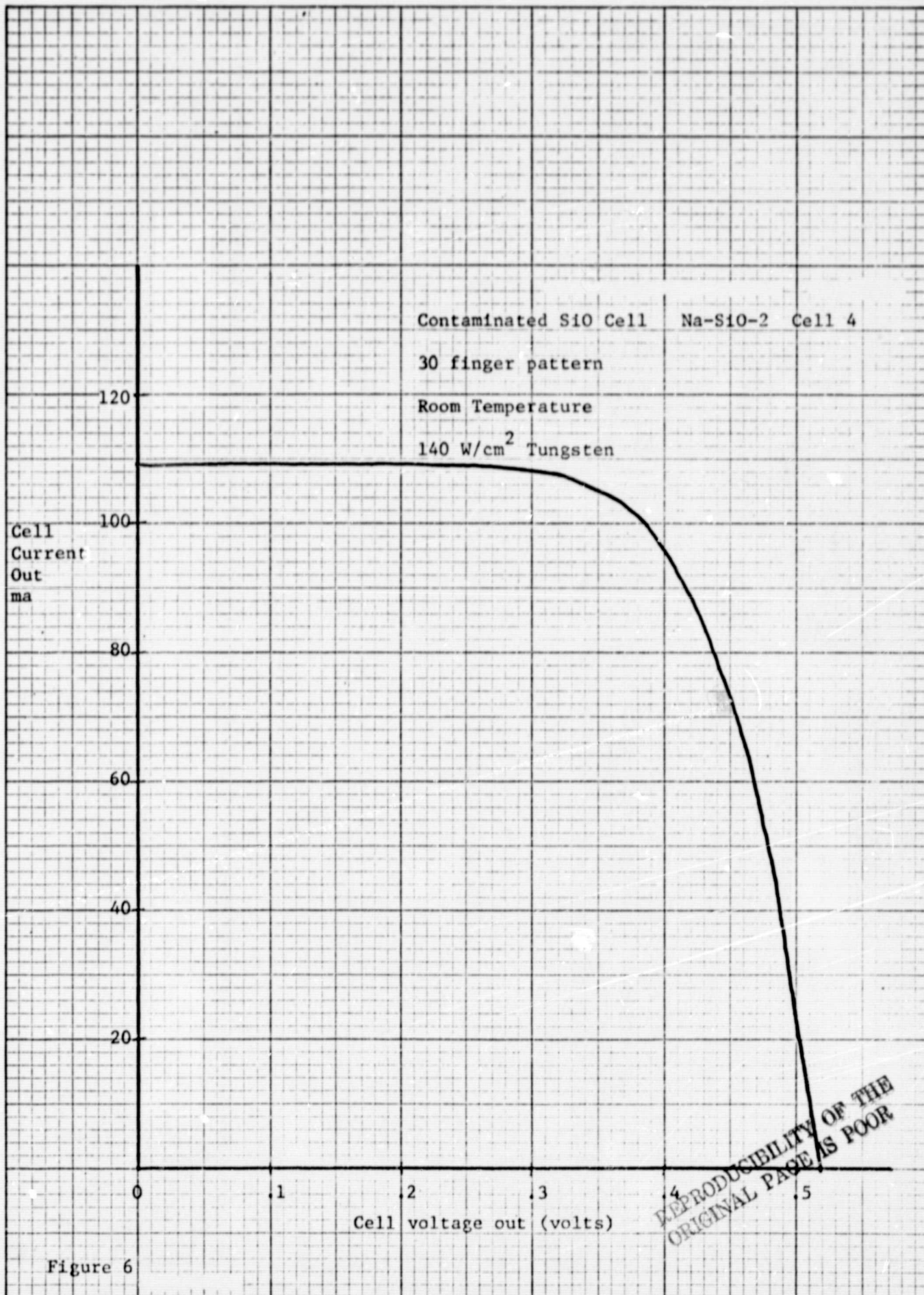
Room Temperature

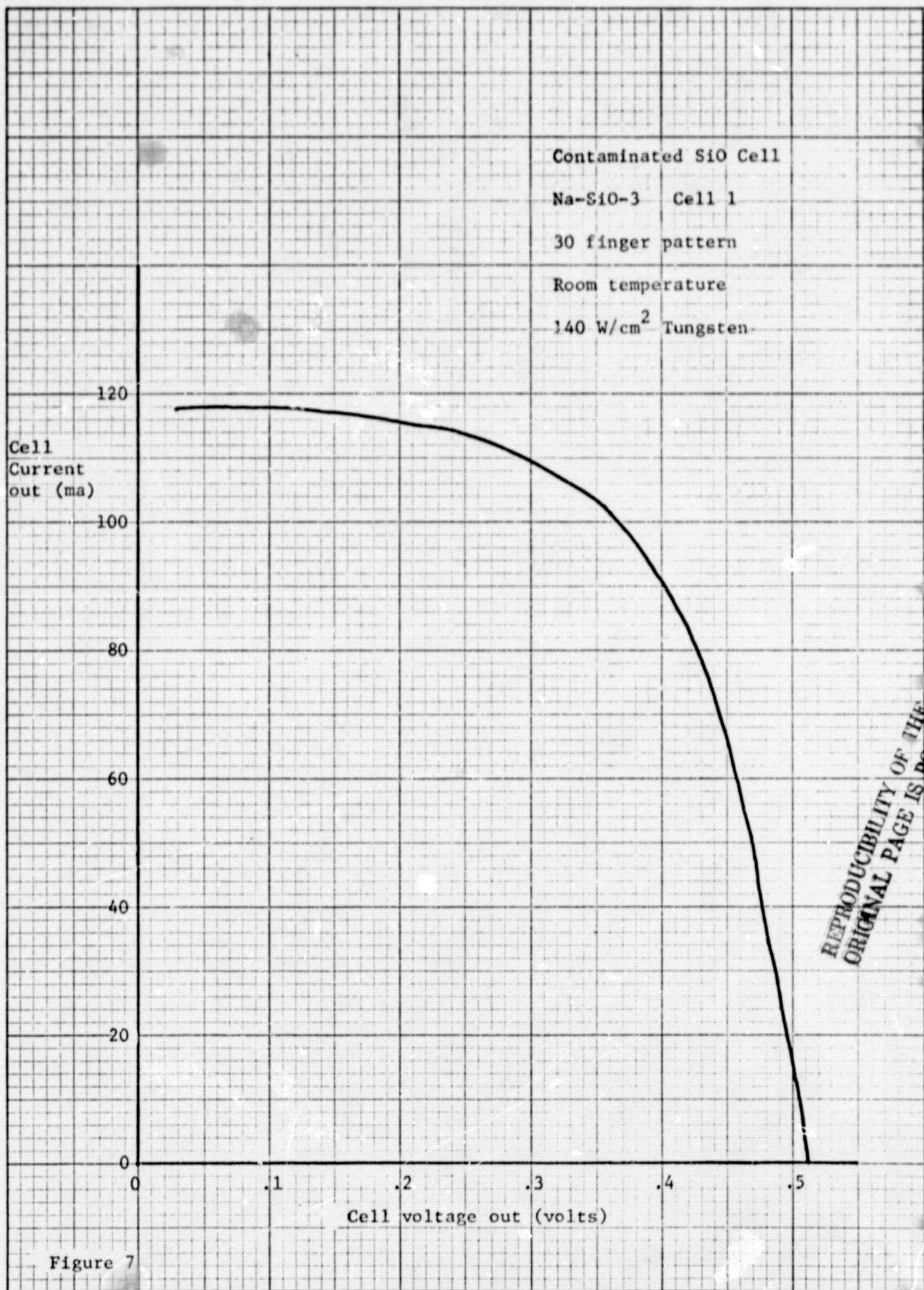
140 W/cm² Tungsten

Cell Voltage Out (Voltage)

Figure 5

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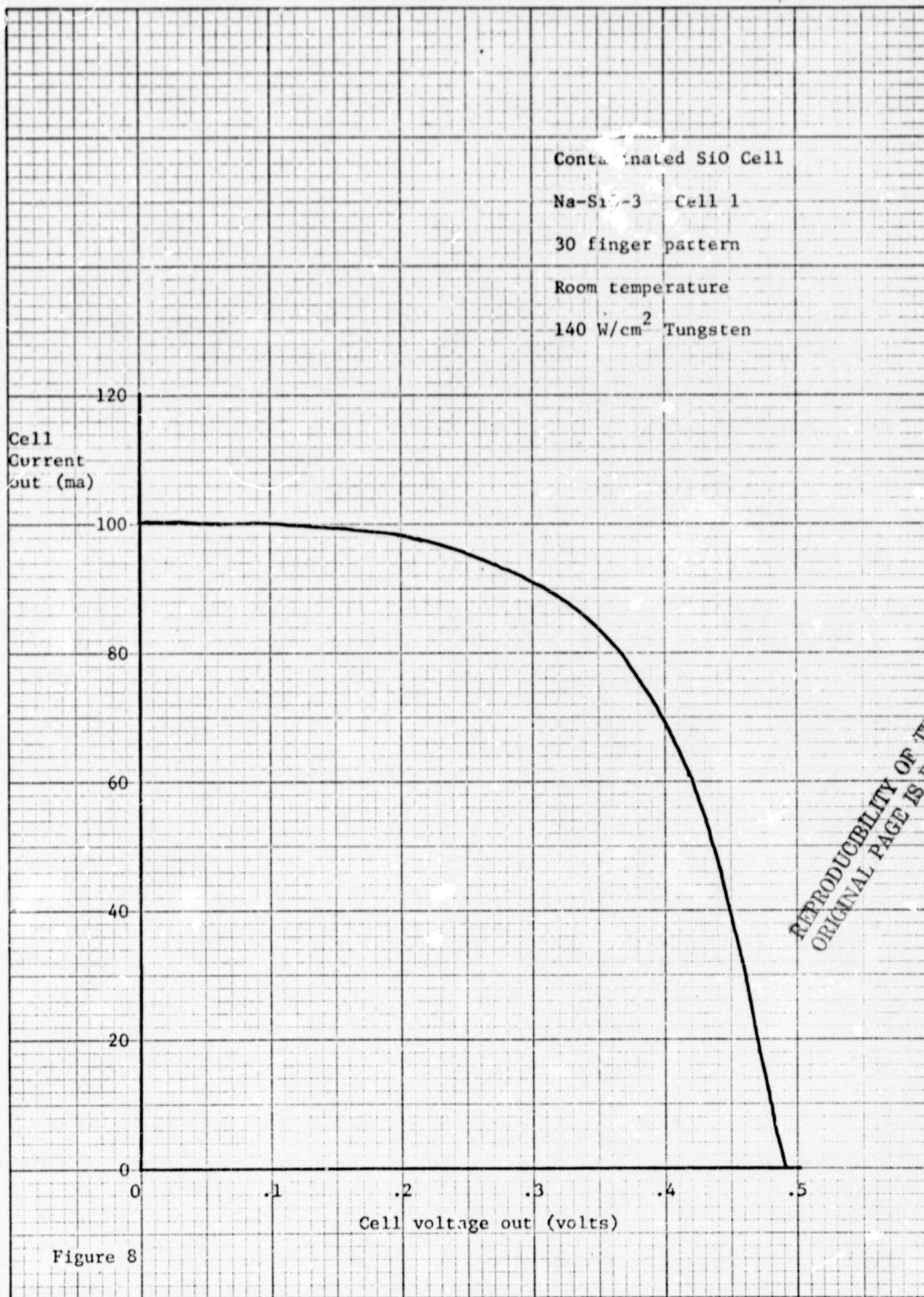


Figure 8

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Na-SiO-4-1

Room Temperature

140 mw/cm^2 incandescent source

I_{sc} - 110 ma

V_{oc} - .51 volts

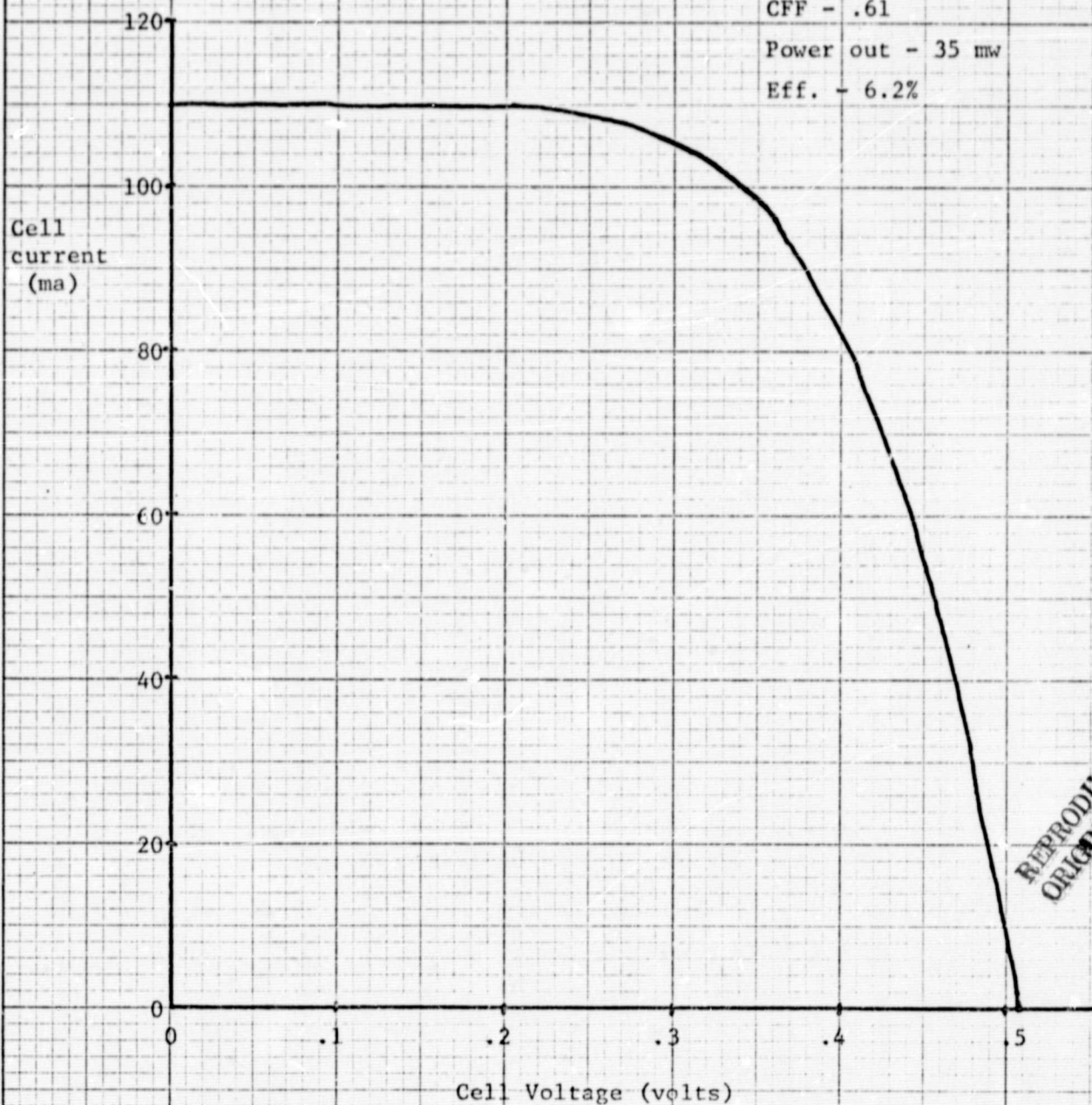
I_{mp} - 93 ma

V_{mp} - .37 volts

CFF - .61

Power out - 35 mw

Eff. - 6.2%



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Fig. 9 Characteristic curve for a sodium contaminated silicon monoxide photovoltaic cell. Na-SiO-4-1

